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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,691	09/15/2003	Teemu Sipila	KOLS.048PA	9770

7590 09/25/2006

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EXAMINER	
ABRAHAM, ESAW T	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 09/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/662,691	SIPILA, TEEMU	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to the applicant's amendment

Applicant's arguments with respect to amended claims 1-18 have been considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Rossman (U.S. PN: 5,027,374).

Specification

In view of the amendment filed on 06/27/06, the examiner withdraws all objections to the specification.

Claim objections

In view of the amendment filed on 06/27/06, the Examiner withdraws all objections to the claims.

Claim Rejections – 35 USC § 112(2nd)

In view of the argument filed 06/27/06, the examiner withdraws the previous 35 USC § 112 rejections.

Status of Claims

1. Claims **1-18** remain pending and new claim (claim 19) is presented for examination,

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims **1-3, 10-11 and 17-18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hosevar et al. (U.S. PN: 6,690,750) in view of Rossman (U.S. PN: 5,027,374).

As per claims 1 and 10:

Hosevar et al. teach or disclose a Viterbi decoder (110) (see FIG. 6) and a method of decoding plurality of trellis stages (see FIG. 5) simultaneously via a cascaded ACS (122) (see FIG. 7 and col. 6 lines 15-30). Further, Hosevar et al. teach that the cascaded ACS (122), in conjunction with the state metric memory (126), determines a set of accumulated state metrics (125), which also referred to as path metrics, for each stage in the trellis as the decoding process moves forward in time and furthermore the cascaded ACS (122) performs additions, subtractions, and

comparisons, with a set of incoming branch metrics (134) and selects new state metrics from which path decision values (124) are determined (see col. 7, lines 19-43). Although, Hosevar et al. in figure 7 disclose four ACS units (150b-156b) connected or coupled to each other (for example, the output of ACS 150b is connected to the input of ACS 152b and the output of ACS 152b is connected to ACS 154b etc..) and this is accomplished by evaluating a metric at each state to determine which one of two incoming branches provides the smallest or preferably largest next state metric (125) depending on the particular algorithm implementation desired (see col. 7, lines 26-31), Hosevar et al. **do not explicitly** teach that the outputs of the ACS units are **directly** connected to the inputs of the ACS units and used in the calculation of the next stage of the trellis. **However,** Rossman in an analogous art teaches a circuit ACS array (comprising ACS units or circuits) connected directly between the ACS circuits in series (see figure 3 elements 20-23) derived from trellis of figure 1 (for example: the output of element 22 is directly connected to the input of element 20 and the output of 20 is directly connected to the input of element 21 etc...(see col. 4, lines 17-33 and claim 5). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the ACS circuits of Hosevar using a direct connection between the ACS circuits as taught by Rossman for calculating trellis next stages. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to in order to calculate new metrics for all states concurrently and therefore has high efficiency and data throughput (see col. 7, lines 17-21).

As per claims 2 and 11:

Hosevar et al. in view of Rossman teach all the subject matter claimed in claim 1 including Hosevar et al. in figure 6 disclose that the cascaded ACS (122) coupled to a SRAM memory (126) for storing the set of metrics which are continually being read out, update and written back thereto (see col. 7, lines 43-50).

As per claim 3:

Hosevar et al. in view of Rossman teach all the subject matter claimed in claim 1 including Hosevar et al. teach that a set of branch metrics are added to the accumulated state metrics from the previous stage then, a branch is chosen from each ACS operation based on which branch will yield the lowest or preferably the highest accumulated state metric for the next stage (see col. 6, last paragraph).

As per claims 17 and 18:

Hosevar et al. in view of Rossman teach all the subject matter claimed in claim 1 including Hosevar et al. in figure 7 disclose four ACS units (150b-156b) connected or coupled directly to each other (for example, the output of ACS 150b is connected to the input of ACS 152b and the output of ACS 152b is connected to ACS 154b etc..) and this is accomplished by evaluating a metric at each state to determine which one of two incoming branches provides the smallest or preferably largest next state metric (125) depending on the particular algorithm implementation desired (see col.7, lines 26-31)

3. Claims **4-9 and 12-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hosevar et al. U.S. PN: 6,690,750) in view of Rossman (U.S. PN: 5,027,374) and further in view of How (U.S. PN: 5,408,502).

As per claims 4 and 12:

Hosevar et al. in view of Rossman teach all the subject matter claimed in claim 1 including Hosevar teaches that the ACS unit (122) forms a cascade and consists of four ACS blocks (150b through 156b) and each ACS block performs a plurality of radix-2 or butterfly ACS (which a butterfly ACS comprises pairs of ACS units) Add/Compare/Select operations over one stage of the trellis (see col.9, lines 19-36). Hosevar et al. **do not explicitly** teach that several ACS units arranged as pair ACS units or ACS banks. **However,** How in FIG. 10 teaches an ACS array, containing eight banks of four ACS pairs wherein Bank (250) (ACS 1), receives the branch metrics output from solid-state switches 210 (BMI), 212 (BMII), 214 (BMIII), and 216 (BMIV) as indicated and Banks 252 (ACS 2), 254 (ACS 3), 256 (ACS 4), 260 (ACS 5), 262 (ACS 6), 264 (ACS 7), and 266 (ACS 8) contain identical ACS pairs, coupled to receive the branch metrics as indicated and further the three lower ACS pairs in each of banks (260, 262, 264 and 266) have their inputs coupled identically with the inputs of the top ACS pair in the respective bank. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Hosevar et al. to arrange or to form ACS units as ACS banks as taught by How. **This modification** would have been obvious because a person having ordinary

skill in the art would have been motivated to in order to reduce bit errors by substantial factor (see col. 13, lines 2-4).

As per claims 5 and 13:

Hosevar et al. in view Rossman and further in view of How teach all the subject matter claimed in claims 1 and 4 including Hosevar et al. teach that the cascaded ACS (122), in conjunction with the state metric memory (126), determines a set of accumulated state metrics (125), which also referred to as path metrics, for each stage in the trellis as the decoding process moves forward in time and furthermore the cascaded ACS (122) performs additions, subtractions, and comparisons, with a set of incoming branch metrics (134) and selects new state metrics from which path decision values (124) are determined (see col. 7, lines 19-43).

As per claims 6 and 14:

Hosevar et al. in view Rossman and further in view of How teach all the subject matter claimed in claims 1 and 4 including How in figure 10 teaches an ACS array, containing eight banks of four ACS pairs wherein Bank (250) (ACS 1), receives the branch metrics output from solid-state switches as indicated and Banks 252 (ACS 2), 254 (ACS 3), 256 (ACS 4), 260 (ACS 5), 262 (ACS 6), 264 (ACS 7), and 266 (ACS 8) contain identical ACS pairs, coupled to receive the branch metrics as indicated and further the three lower ACS pairs in each of banks (260, 262, 264 and 266) have their inputs coupled identically with the inputs of the top ACS pair (in parallel) in the respective bank.

As per claims 7 and 15:

Hosevar et al. in view of Rossman and further in view of How teach all the subject matter claimed in claims 1 and 4 including Hosevar et al. in figure 7 disclose four ACS units (150b-156b) connected or coupled directly to each other (for example, the output of ACS 150b is connected to the input of ACS 152b and the output of ACS 152b is connected to ACS 154b etc.) and this is accomplished by evaluating a metric at each state to determine which one of two incoming branches provides the smallest or preferably largest next state metric (125) depending on the particular algorithm implementation desired (see col.7, lines 26-31). Further, Hosevar et al. in figure 6 teaches that the input to cascaded ACS unit (122) fed back from the output of the cascaded ACS unit via the state metric memory (126).

As per claims 8, 9, and 16:

Hosevar et al. in view of Rossman and further in view of How teach all the subject matter claimed in claims 1 and 4 including Hosevar et al. teach a VLSI architecture for a Viterbi decoder for wireless or other type applications which may operate within a programmable DSP system (processor)(see col. 4, lines 37-44). Further, Hosevar et al. teach all the subject matter claimed in claim 1 including Hosevar et al. in figure 6 disclose that the cascaded ACS (122) coupled to a SRAM memory (126) for storing the set of metrics which are continually being read out, update and written back thereto (see col. 7, lines 43-50).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,111,835 Honama

US PN:7,020,827 Gatherer et al.

5. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for after final communications.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

Esaw Abraham

Art unit: 2133

GUY LAMARRE
PRIMARY EXAMINER